Amendments of the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the above-identified patent application:

Listing of Claims

1. (currently amended) Circuitry for using a reference clock signal to extract data from a data signal, the data signal having a data rate that is twice the reference clock signal frequency, comprising:

first circuitry configured to derive from the reference clock signal first and second phase-shifted versions of the reference clock signal that are respectively synchronized with oppositely polarized transitions in level of the data signal;

second circuitry configured to sample the data signal in a predetermined phase relationship to the first phase-shifted version of the reference clock signal in order to produce a first partial stream of data extracted from the data signal; and

third circuitry configured to sample the data signal in a predetermined phase relationship to the second phase-shifted version of the reference clock signal, while the second circuitry samples the data signal in a predetermined phase relationship to the first phase-shifted version of the reference clock signal, in order to produce a second partial stream of data extracted from the data signal.

2. (original) The circuitry defined in claim 1 wherein the first circuitry comprises:

fourth circuitry configured to produce a plurality of more than two phase-shifted candidate versions of the reference clock signal.

3. (original) The circuitry defined in claim 2 wherein the first circuitry further comprises:

fifth circuitry configured to select from the candidate versions first and second candidate versions that are most nearly in phase with transitions in the level of the data signal having a first polarity; and

sixth circuitry configured to select from the candidate versions third and fourth candidate versions that are most nearly in phase with transitions in the level of the data signal having a second polarity.

4. (original) The circuitry defined in claim 3 wherein the fifth circuitry comprises:

seventh circuitry configured to interpolate between the first and second candidate versions to produce the first phase-shifted version of the reference clock signal.

5. (previously presented) The circuitry defined in claim 3 wherein the fifth circuitry comprises:

seventh circuitry configured to select the one of the first and second candidate versions that is closer in phase with transitions in the level of the data signal having a first polarity as the first phase-shifted version of the reference clock signal.

6. (previously presented) The circuitry defined in claim 1 further comprising:

first multi-stage shift register circuitry having a data input terminal to which the first partial data stream is applied, the first shift register circuitry being configured to shift in data from its input terminal in a predetermined phase relationship to the first phase-shifted version of the reference clock signal.

7. (original) The circuitry defined in claim 6 further comprising:

first shift register reading circuitry configured to read out in parallel the contents of multiple stages of the first shift register circuitry.

8. (previously presented) The circuitry defined in claim 7 wherein the first shift register reading circuitry is configured to operate in a predetermined phase relationship to the first phase-shifted version of the reference clock signal.

9. (previously presented) The circuitry defined in claim 8 wherein the first shift register reading circuitry is further configured to operate in response to only a selected fraction of cycles of the first phase-shifted version of the reference clock signal.

10. (original) The circuitry defined in claim 9 wherein the fraction is programmably selectable.

11. (original) Programmable logic device circuitry comprising:

circuitry as defined in claim 1.

12. (original) A digital signal processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

programmable logic device circuitry as defined in claim 11.

13. (original) A printed circuit board on which is mounted programmable logic device circuitry as defined in claim 11.

14. (original) The printed circuit board defined in claim 13 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device circuitry.

15. (original) The printed circuit board defined in claim 13 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device circuitry.

16. (currently amended) A method of extracting data from a data signal having a predetermined data rate comprising:

providing a reference clock signal having a frequency that is one-half the data rate;

deriving from the reference clock signal first and second versions of that signal that are respectively synchronized with oppositely polarized transitions in level of the data signal;

producing a first partial stream of data extracted from the data signal by sampling the data signal in a predetermined phase relationship to the first phase-shifted version; and

producing a second partial stream of data extracted from the data signal by sampling the data signal in a predetermined phase relationship to the second phase shifted version, while the first partial stream of data is being extracted from the data signal by sampling the data signal in a predetermined phase relationship to the first phase-shifted version.

17. (original) The method defined in claim 16 wherein the deriving comprises:

producing from the reference clock signal a plurality of more than two phase-shifted candidate versions of the reference clock signal.

18. (original) The method defined in claim 17 wherein the phase shifts of the candidate versions equally divide among them a cycle of the reference clock signal.

19. (previously presented) The method defined in claim 17 wherein the deriving further comprises:

selecting the first and second candidate versions that are most nearly in phase with transitions in the level of the data signal having a first polarity.

20. (original) The method defined in claim 19 wherein the deriving further comprises:

interpolating between the first and second candidate versions to produce the first phase-shifted version of the reference clock signal.

21. (original) The method defined in claim 19 wherein the deriving further comprises:

selecting as the first phase-shifted version of the reference clock signal the one of the first and second candidate versions that is closer in phase with transitions in the level of the data signal having the first polarity.

22. (original) The method defined in claim 16 further comprising:

shifting the first partial stream of data into the stages of a multi-stage shift register in a predetermined phase relationship to the first phase-shifted version.

23. (original) The method defined in claim 22 further comprising:

periodically reading out in parallel the contents of multiple ones of the shift register stages.

24. (previously presented) The method defined in claim 16 wherein the providing comprises:

operating phase locked loop circuitry to produce the reference clock signal.

25. (currently amended) Apparatus for receiving an information signal that includes data information and clock information for the data information embedded in the information signal comprising:

first input circuitry configured to receive the information signal;

second input circuitry configured to receive a reference clock signal having a reference frequency which is related to a frequency of the clock information by a predetermined scale factor;

reference clock signal processing circuitry configured to use the information signal and the reference clock signal to produce two recovered clock signals, where each recovered clock signal has a respective one of two shifted phases, each of which corresponds to a phase of the clock information, where each recovered clock signal has a frequency that is half a frequency of the clock information, and where each recovered clock signal is respectively synchronized with oppositely polarized transitions in level of the information signal; and

data recovery circuitry configured to use the two recovered clock signals and the information signal to produce two retimed data output signals indicative of the data information in the information signal, one of the two retimed data output signals being produced using a first respective recovered clock signal while the other of the two retimed data output signals is being produced using a second respective recovered clock signal.

26. (original) The apparatus defined in claim 25 wherein the reference clock signal processing circuitry comprises:

first phase locked loop circuitry configured to use the reference clock signal and the scale factor to produce a plurality of candidate further reference clock signals, each further reference clock signal having a frequency that is half a frequency of the clock information and having a phase which is different from the phases of all the other candidate further reference clock signals.

27. (original) The apparatus defined in claim 26 further comprising restoring circuitry to restore the plurality of candidate further reference clock cycles to a duty cycle of 50/50.

28. (original) The apparatus defined in claim 27 further comprising a multiplexer configured to select a plurality of candidate further reference clock cycles from one of the first phase locked loop circuitry and the restoring circuitry.

29. (original) The apparatus defined in claim 28 further comprising further phase locked circuitry configured to use the information signal and the candidate further reference clock signals to produce the two recovered clock signals.

30. (original) The apparatus defined in claim 29 wherein the further phase locked loop circuitry comprises:

selection circuitry configured to select as the two recovered clock signals two of the candidate further reference clock signals having the phase that works best with the phase of the clock information.

31. (original) The apparatus defined in claim 26 wherein the reference clock signal processing circuitry further comprises:

second phase locked loop circuitry configured to use the reference clock signal and the scale factor to

produce a plurality of candidate further reference clock signals, each further reference clock signal having a frequency that is half a frequency of the clock information and having a phase which is different from the phases of all the other candidate further reference clock signals, wherein the second phase locked loop circuitry has a range of frequencies different from the first phase locked loop circuitry.

32. (original) The apparatus defined in claim 31 further comprising a multiplexer configured to select a plurality of candidate further reference clock signals from one of the first phase locked loop circuitry and the second phase locked loop circuitry.

33. (original) The apparatus defined in claim 25 wherein the data recovery circuitry comprises:

first multi-stage shift register circuitry configured to shift in a first retimed data output signal in a predetermined phase relationship to a first recovered clock signal; and

second multi-stage shift register circuitry configured to shift in a second retimed data output signal in a predetermined phase relationship to a second recovered clock signal.

34. (original) The apparatus defined in claim 33 further comprising:

first shift register reading circuitry configured to read out in parallel contents of multiple stages of the first shift register circuitry; and

second shift register reading circuitry configured to read out in parallel contents of multiple stages of the second shift register circuitry.

35. (original) The apparatus defined in claim 34 further comprising:

programmable divider circuitry configured to divide one of the two recovered clock signals by a programmable factor to produce a reference clock signal; and

multi-stage parallel buffer register circuitry configured to read in parallel contents of multiple stages of the first and second shift register circuitry and to unload all stages of the first and second shift register circuitry in parallel in synchronism with the reference clock signal.

36. (previously presented) The apparatus defined in claim 35 further comprising:

synchronizer circuitry configured to convert the parallel data output signal to a further data output signal synchronized with a read control signal which can have a phase and frequency substantially unrelated to the phase and frequency of the reference clock.

37. (original) The apparatus defined in claim 36 further comprising:

selection circuitry configured to select as a final data output signal either the parallel data output signal or the further data output signal.